Vers un changement de paradigme dans l’utilisation de la mémoire ?

Christophe MULLER
Im2np – UMR CNRS 7334
Polytech’ Marseille, Aix-Marseille Université
Technopôle de Château–Gombert
13451 Marseille Cedex 20

e–mail : christophe.muller@im2np.fr

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Outline

1. Memory Taxonomy

2. Resistive Memory Technologies
   • MRAM – Magnetoresistive RAM
   • PCM – Phase Change RAM
   • RRAM – Redox RAM

3. Embedded Non-Volatile Memories

4. New paradigms
   • Distributed Memory in Logic
   • Biomimetic Architectures

5. Concluding Remarks
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Memory Taxonomy

**Memories**

- **Volatile**
  - DRAM (Micron)
  - SRAM

- **Non-volatile**
  - Charge storage
    - EEPROM, Flash, FRAM, Si-dots
  - Resistance switching
    - MRAM, PCM, RRAM

**Examples**

- DRAM (Micron)
- Copper M3
- Copper M2
- Flash (Intel)
- (MRAM) Freescale
Universal Memory: the Holy Grail?

• Memory simultaneously combining...
  ▪ Density > GBytes
  ▪ Endurance > $10^{15}$ cycles ("infinite")
  ▪ Operation voltage compliant with CMOS $V_{dd}$
  ▪ Read/write access times of few nanoseconds
  ▪ Low power consumption (< 1 pJ/bit)
  ▪ Retention > 10 years

• … and supporting a downsizing of its critical dimensions
  ▪ Suited for leading edge technology node

Some specifications may be relaxed depending on the application requirements…
Key Requirements for Alternative NVM

- Readiness for leading edge technology node
- Cost structure
  - MLC (Multi Levels Cell) capable
  - BEOL (Back-End Of Line) compatible and 3D stackable
- Scalability
  - In x and y with lithography
  - In z with number of layers
- Performances
  - Low power
  - Flexibility
- Reliability
  - Non-volatility with long retention (> 10 years)
  - High endurance
Flash Scaling Issues

- Full glass = 0
- Empty glass = 1

- Mono-electron effects
- Electrostatic coupling
- Non-scalable dielectrics...

Alternative solutions are required!

Deleruyelle et al., Solid State Electronics, vol. 49, no. 11, p. 1728, 2005
The Race of Emerging Technologies

Memory cell size ($F^2$)

- MRAM
- FRAM
- Flash NOR
- Flash NAND
- PCM
- RRAM ?

Technology (nm)
Many Players on Resistance Switching*

*Non-exhaustive list…
# Global Market for Alternative NVM*

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<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>North America</td>
<td>48</td>
<td>684</td>
<td>+70%</td>
</tr>
<tr>
<td>Europe</td>
<td>46</td>
<td>620</td>
<td>+68%</td>
</tr>
<tr>
<td>Rest of World</td>
<td>21</td>
<td>286</td>
<td>+69%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>115</strong></td>
<td><strong>1,590</strong></td>
<td><strong>+69%</strong></td>
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* 7 technologies: FRAM, MRAM, PCM, RRAM, ZRAM, quantum dots & polymer

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Potential Markets

• **MRAM**
  - Applications requiring Flash-like non volatility, SRAM-like fast nanosecond switching and DRAM-like infinite endurance
  - Replacement of SRAM/Flash combos and battery-backup RAM

• **PCM**
  - Most advanced technology (process maturity, storage capacity)
  - Highest market share in 2015 (*iRAP* projection)
  - Positioned as a NOR-Flash substitute

• **RRAM**
  - Technology still in its "infancy"
  - Promising for high density storage with possibly 3D architecture
  - Market yet to be defined: NAND/DRAM replacement?
Spintronics

- Electron has...
  - ...an electrical charge ⇒ "Microelectronic"
  - .... and a spin ⇒ Spin electronics or "spintronics"

- Spin electronics is....
  - Intrinsically non volatile
  - Potentially very fast (f > GHz)
  - Shown to be scalable (in data storage)
Analogy
Tunneling
• Devices relying on Tunnel Magneto Resistance (TMR)
  - Interaction between electron spin and magnetization of ferromagnetic (FM) layers
  - Resistance depends upon respective magnetization orientations of FM layers separating tunnel oxide
  - Field-induced magnetic switching (FIMS)
Conventional Design (FIMS)

Addressed magnetic tunnel junction (MTJ)

1T/1MTJ unit cell

Conventional parallel-NOR architecture

US Patents no. 6,331,943 – 6,806,523 – 7,411,816
Different MRAM Flavors

- Enhanced immunity to bit fail during writing

Toggle switching

<table>
<thead>
<tr>
<th>Top electrode</th>
<th>Free SAF</th>
<th>Ru</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Tunnel barrier</td>
<td>AIOx</td>
</tr>
<tr>
<td>Sense layer</td>
<td>Reference layer</td>
<td></td>
</tr>
<tr>
<td>Pinning</td>
<td>Base electrode</td>
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Thermally Assisted Switching

Available Chips in 2013?

- Everspin MRAM (16 Mb)

≈ 20 firms actively pursuing efforts on MRAM development

**Toggle MRAM**
- 180 nm CMOS technology
- Memory blocks: 16 × 1 Mbit
- Supply voltage: 3.3 V
- Speed: 35 ns
Future Solutions?

- 4Mb 2006
- 16Mb 2010
- Mb → Gb
- STT, MLC?
- Mb → Gb

Toggle, TAS
Spin Torque Transfer, STT

- Magnetization reversal achieved through injection of spin polarized current in MTJ
  - Simple architecture without "field lines"
  - High scalability (20-30 $F^2$ for FIMS $\rightarrow$ 6 $F^2$ for STT)
  - Excellent write selectivity
  - Low power consumption (write current < 100 µA)

Multi Levels Cell, MLC

- MLC STT memory (2 bits per cell) demonstrated by Hitachi and University of Tohoku
  - 2 series MTJs (with different areas)
  - Four-level operations achieved by spin torque transfer
  - Effective area of memory cell per bit < 4 $F^2$
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Analogy: Silicon Dioxide $\text{SiO}_2$

**Glass (silica)**
- Disordered amorphous phase

**Quartz**
- Ordered crystalline phase

Reversible phase transition
**Prototypical Material**

- **Chalcogenide alloy (GST = Ge$_2$Sb$_2$Te$_5$)**
  - Reversible transition between crystalline and amorphous states
  - Resistance switching between two distinct resistance states
    - ✓ Crystalline phase $\rightarrow R_{\text{Low}}$
    - ✓ Amorphous phase $\rightarrow R_{\text{High}}$
Downscaling

As the PCM memory cell shrinks, the programmable volume shrinks. Smaller programmable volume translates into better performing PCM devices.
Available Chips in 2013?

Omneo PCM (128 Mb)

PRAM (512 Mb)

Dec. 2012. Micron has announced it has been shipping 45 nm 1 Gbit PCM multichip package to Nokia

Villa et al., IEEE Proc. of ISSCC 2010 (Micron, former Numonyx)

Chung et al., IEEE Proc. of ISSCC 2011 (Samsung)
Conventional Design

- **Access device** (= selector)
  - MOSFET transistor, BJT or diode

Architecture implementing 1 access device/1R memory cells
**Main Issues**

- **Temperature**
  - $T_M$: Reset operation
  - $T_X$: Set operation

- **State**
  - Amorphous State "0"
  - Crystalline State "1"

- **Liquid**

- **Thermal stability**
  - "New" materials
  - Downward arrow: Retention

- **High reset current**
  - Downward arrow: Power consumption
  - Innovative architectures

- **Thermal spread**
  - Downward arrow: Memory density
  - Confined PCM volume

- **Main Issues**
  - High reset current
  - Power consumption
  - Innovative architectures
Towards Confined Structures

• Advantages of confinement
  ▪ ↓ Melting temperature
  ▪ ↓ Reset current

• Process challenges
  ▪ Sputtering → CVD (conformal dep.)
  ▪ Etching recipes
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Many Different Memory Stacks

**Unipolar switching**

- Fujitsu (doped NiO)
- Samsung (NiO)
- Matsushita (FeO$_x$)

**Bipolar switching**

- Adesto Technologies
- HP Labs
- Rambus (former Unity)
Analogy: Fuse/Antifuse
Filamentary Unipolar Switching

- Local reduction process leading to the formation of conductive filaments (CFs)
- Thermal dissolution of conductive filaments (CFs)

Typical unipolar I(V) characteristic
Manipulating Filaments at Nanoscale

- Voltage controlled creation and dissolution of nanosized filaments
  - Forming, set and reset operations at nanoscale

![Diagram of filament manipulation](image)

Nardi et al., Journal of Applied Physics, vol. 112, pp. 064310(1–6), 2012
Conventional Design

- Integration of simple MIM capacitors into BEOL
  - Possibly 3D cross-bar memory architectures
Cross-Bar with Selector (Unipolar)

- Select device required to avoid parasitic paths (as PCM)
  - MOSFET transistor or diode

With $n$ layer stack, effective cell size is $(4/n) F^2$
Available Chips in 2012?

January 2012
Japanese memory specialist Elpida has announced the development of a resistance memory (ReRAM) prototype, which it claims paves the way for high-speed non-volatile storage that combines the best of DRAM and NAND flash technologies.

December 2011
Elpida, Hynix, IMEC, Micron, Panasonic, Samsung, Sharp and others are working on ReRAM. In fact, Micron and Sony Corp. have quietly forged an alliance in ReRAM. “Micron and Sony have entered into a joint development program to co-develop a new non-volatile memory focused on a conductive bridge-type random access memory, ReRAM”.

None currently, despite many announcements...

February 2012
Flash memory vendor SanDisk Corp. is looking for a director of processing engineering management for a 3D resistive RAM team based in Milpitas. [...] According to the advertisement, the individual will manage a team of about 30 engineers that is working to develop ReRAM switching material, a selector device and associated technology that can be manufactured with "acceptable 3-D product yield, reliability and performance".

June 2011
Adesto Technologies Corp., a startup company developing conductive bridging RAM nonvolatile memory technology, has announced that it will ship products this year manufactured by foundry partner Altis Semiconductor SA.

IMEC, IEDM, December 2011
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Generic Resistive Memory Circuit

- Generic resistive switching memory circuit
  - Core-cell relies on the association of a select/access device (to avoid parasitic paths) with a resistor
  - 1T/1R core-cell

Data Discrimination

- Statistical distributions of high and low resistances
  - Memory window

![Diagram showing statistical distributions of high and low resistances]

- Narrow distributions but small $\Delta R$
- Large $\Delta R$ but wide distributions
Satisfactory Memory Window

- Data discrimination requires distinct resistance states with $R_{\text{Low}}$ as large as possible (↓ power consumption)
  - Material optimization (→ higher $R_{\text{Low}}$)
  - Limited process variations (→ narrow resistance distributions)
  - Novel memory cells (with ad hoc physical modeling)
  - Innovative architectures...

\[ \Delta R = R_{\text{High}} - R_{\text{Low}} \]

Unambiguous discrimination

Cell-to-Cell Variability

- Bipolar resistive switching memories
  - Physical model calibrated on actual electrical data \(^1\)
  - Monte-Carlo simulation of \(3 \times 3\) bits memory array (1T/1R cells) \(^2\)
  - Impact on set and reset operations

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2 Aziza et al., IEEE Proc. of Non-Volatile Memory Technology Symposium, 2011
Impact of Routing Circuitry

- Influence of parasitic on bipolar I(V) curves
  - Resistive paths (50 to 500 Ω)
  - BL/WL capacitive coupling (0.1 to 1 pF)

- Strong influence of resistive paths
  - $R_{\text{Low}} \gg R_{\text{wires}}$
  - $R_{\text{Low}}$ controlled by set current

- No effect of capacitive coupling

Aziza et al., IEEE Proc. of International Design and Test Workshop, pp. 78-81, 2011
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Design Challenges

• Interconnected chips
  ▪ Separate optimized technologies
  ▪ Tradeoffs: cost, communication speed

• Embedded implementation
  ▪ Logic and NVM on a monolithic substrate
  ▪ Tradeoffs: process compatibility, poor array efficiency, communication speed

• Distributed implementation
  ▪ Single chip with distributed NVM circuits
  ▪ Challenges: low cost, BEOL compatible, low power and low voltage NVM elements
Bottlenecks

• Control of underlying technology
  - Cell to cell process variability
  - Suitable performances

• Understanding of physical mechanisms
  - Programming operations
  - Reliability

• Development of device models
  - Physical and compact models
  - Scaling limits

• Novel circuit design techniques
  - Distributed cells
  - Biomimetic architectures
New Paradigms

Today

SRAM cache
Analog FE
LV Logic
CPU
HV Logic
NOR NVM
NAND NVM

Tomorrow?

Embedded Resistive Switching Memory

Evolution driven by low power and low cost
Memristor Mimicking Brain Synapse

• Memristor: short for "Memory resistor"
  ▪ 4th electrical element defined by L. Chua¹ (Berkeley Univ.) in 1971 for electrical circuits
  ▪ Bipolar oxide-based resistive stack demonstrated by HP²

• Human brain-like characteristics
  ▪ Memristor could lead to computer systems that can remember and associate patterns in a way similar to how people do

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Concluding Remarks

• Mainstream non-volatile memory (Flash) is today approaching its scaling limits
• "Nano" materials evolution or revolutions have paved the way towards new memory concepts
  ▪ Several alternative concepts have been proposed
  ▪ Few of them are really appealing from a cost standpoint
• For memory circuits, crossbar 3D approach is identified to further reduce the cost/bit
• New trends beyond conventional memory
  ▪ Logic coupled with memory
  ▪ Distributed NVM cells architectures for ULP applications
  ▪ Biomimetic architectures
Interdisciplinary Approach

Whatever the technology, the development of emerging memory concepts emphasizes the necessity to make stronger links between memory cell materials, physical mechanisms, modeling and circuit design.
Thank You for Your Attention

Institut Matériaux Microélectronique Nanosciences de Provence
UMR 7334 CNRS, Universités Aix-Marseille et Sud Toulon-Var

"Vieux port" of Marseille

christophe.muller@im2np.fr